REMARKS

The present Amendment is in response to the Office Action having a mailing date of January 27, 2005. Claims 1-19 are pending in the present Application. Claims 1-19 are rejected. Claims 1, 13, and 15 have been amended to further define the scope and novelty of the present invention, to place the claims in condition for allowance. Support for the amendments to the claims is found throughout the specification, and in particular, on page 4, lines 7-10; page 11, lines 17-18; and page 12, lines 8-11. Applicants respectfully submit that no new matter has been presented. Consequently, claims 1-19 remain pending in the present application. For the reasons set forth more fully below, Applicants respectfully submit that the claims as presented are allowable. Consequently, reconsideration, allowance, and passage to issue are respectfully requested.

Present Invention

An application specific integrated circuit (ASIC) is disclosed. The ASIC includes a standard cell. The standard cell includes a plurality of logic functions. The ASIC also includes at least one bus coupled to at least a portion of the logic functions and a plurality of internal signals from the plurality of logic functions. Finally, the ASIC includes a filed programmable (FP) function coupled to the at least one bus and at least a portion of the plurality of internal signals. The FP function provides access to internal signals for observation and control without requiring input/output (I/O) pins to access the internal signals.

An ASIC using a filed programmable gate array (FPGA) function within a standard cell design is utilized to create an internal-to-the-ASIC bridging of internal signals to observe and control of the internal signals of the ASIC. By the placement of the logic, which expresses a test

program into the FPGA function and manipulates the I/O pins and/or other functional entities of interest, the ASIC function and/or surrounding logic can be easily verified. In addition, through this system, internal and/or system (external-to-the ASIC) conditions can be observed. Furthermore, a sequence of resets to different functional blocks can be executed utilizing a system and method in accordance with the present invention. Finally, through this system the end user of the ASIC could write their own error condition correction FPGA code which would communicate using protocols of the existing system error condition architecture.

Claim Rejections - 35 U.S.C. §102

The Examiner has stated:

Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Shen et al. U.S. Patent No. 6,829,751.

As per claim 1, Shen et al. teaches providing a method and/or architecture for implementing a diagnostic architecture using an (*field programmable function*) FPGA core in a system on-chip design that can (i) ease bringing up, verification and debugging by providing interconnection and programming options; (ii) *observe* important signals while the chip is running under a normal mode; (iii) run at a single step mode while under the control of the FPGA core; (iv)display appropriate signals on a debugging workstation, allowing many debugging features to be supported such as: (a) triggering and tracing based on *internal signals*, (b) dynamically changing host register values and (c) providing complex monitoring functions (*observation and control*), since the (*field programmable function*) FPGA is programmed; (v) reduce debugging/verification time and/or (vi) improve product time to market. (Column 1 line 56 through column 2 line 12) The register block communicates with the FPGA core through a bus (*at least one bus coupled to at least a portion of the logic functions*). Similarly, the register block (*standard cell*) can also communicate with the FPGA core through other busses. The buses can be implemented as multi-bit buses or can also be implemented as single bit buses, if appropriate. Additionally, the buses can also be implemented as bidirectional buses. The FPGA core can communicate with the control block (*standard cell*) through a bus. The FPGA core can communicate through a number of I/O pins over a bus. (Fig 2, column 3 lines 13-31) By using the FPGA core to implement such chip diagnostics, simultaneous probing of internal signals can be achieved while the system is running under predetermined conditions (e.g., a normal mode of operation). (Column 3 lines 32-42 figure 2) This circuit can also be implemented by the preparation of (*application specific integrated circuit*) ASICS, FPGAs, or by interconnecting an appropriate network of conventional component circuits. (Column 5 lines 54-58) The circuit can provide a FPGA core in an ASIC architecture that eases chip bring up, verification and debugging by

interconnection and programming options. This allows important signals of a chip to be observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O. This allow all the signals of the chip to be displayed while the chip is running under a single step mode by allowing a FPGA core to control the chip. (Column 6 lines 18-30)...

Applicant respectfully disagrees with the Examiner's rejections. Shen discloses diagnostic architecture using a FPGA core in a system-on-a-chip design. The architecture includes a system for designing an integrated circuit (IC). The system includes a circuit and a programmable portion used for diagnostics and finding bugs. The circuit includes a functional portion and a logic portion that may be connected to the functional portion. The logic portion includes one or more interfaces. The programmable portion may be configured to detect, correct and/or diagnose errors in the logic portion through the one or more interfaces. Up to 1K of internal signal probing can be supported simply by directly connecting the signal to the I/O_PINS of the FPGA core. Also, important signals of a chip can be observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O. (Column 3, lines 58-61, column 6, lines 25-29, and the Abstract.)

However, Shen does not teach or suggest monitoring internal signals "without requiring input/output (I/O) pins to access the internal signals," as recited in amended independent claims 1, 13, and 15. Instead, Shen explicitly teaches that "up to 1K of internal signal probing can be supported simply by directly connecting the signal to the I/O_PINS of the FPGA core" (column 3, lines 58-61). Furthermore, while Shen teaches simultaneously probing multiple internal signals by utilizing a scan chain (column 6, lines 45-47), Shen also teaches that when collecting data using the scan chain, the "I/O interface may then transfer the data to the debugging workstation" (column 4, lines 55-58). Shen further states that "software can display any of the internal signals that are connected to the I/O of the FPGA core" (column 5, lines 33-36), and that

important signals of a chip can be "observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O" (column 6, lines 25-29). In other words, Shen requires I/Os in order to debug internal signals using the debugging workstation, to display internal signals using software, and/or to observe internal signals. Nowhere does Shen teach or suggest monitoring internal signals "without requiring input/output (I/O) pins to access the internal signals," as recited in the present invention.

Therefore, Shen does not teach or suggest the present invention as recited in amended independent claims 1, 13, and 15, and these claims are allowable over Shen.

Dependent claims

Dependent claims 2-12, 14, and 16-19 depend from amended independent claims 1, 13, and 15, respectively. Accordingly, the above-articulated arguments related to amended independent claims 1, 13, and 15 apply with equal force to claims 2-12, 14, and 16-19, which are thus allowable over the cited reference for at least the same reasons as claims 1, 13, and 15.

Conclusion

In view of the foregoing, Applicants submit that claims 1-19 are patentable over the cited reference. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes that this application is in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

April 27, 2005
Date

Joseph A. Sawyer, Jr.
Attorney for Applicant(s)
Reg. No. 30,801
(650) 493-4540